

A 16 X 16 PROGRAMMABLE POISSON-EQUATION SOLVER IMPLEMENTED IN ANALOG VLSI

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Abstract

This work describes a proto-type system that solves Poisson's equation using massively parallel analog circuits. The system contains a rectangular array of 16 x 16 cells, each cell measuring 100 μm x 100 μm in a 1.2- μm process. Cells connect to four nearest neighbors via complementary MOS transistors operating in the ohmic region. Each boundary cell has a programmable voltage source, while each interior cell has a programmable current source. Data from a static 8 x 8 Poisson equation solver chip demonstrates the feasibility of our design.

1. Introduction

The purpose of the programmable Poisson-equation solver is to estimate the phase of a wavefront. Depending on the application, several types of sensors can be used to infer the phase of an incoming wavefront. An example is the Hartman sensor, which is shown in Fig. 1. The Hartman sensor detects the slope of an aberrated wavefront by measuring the centroid in a small region of the image [1]. The derivatives of these centroid measurements, together with appropriate boundary conditions, are used as inputs to the Poisson-equation solver to back out the phase.

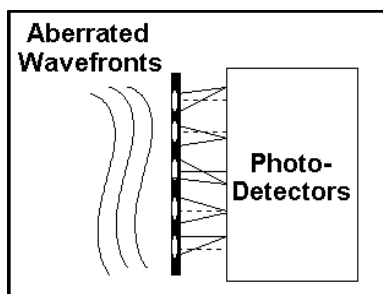


Figure 1 Hartman sensor.

Poisson's equation is typically solved using finite element analysis, which divides a continuous region into

a set of discrete points. In this work, we use an analog VLSI circuit to solve Poisson's equations using massively-parallel, micro-power analog circuits. The architecture of the solver is a rectangular array of uniform resistive elements. In order to save area and to achieve programmability, resistive elements are implemented as complementary MOS transistors operating in the ohmic region.

2. Circuit Description

The floorplan of the Poisson-equation solver is shown in Fig. 2 and resembles that of a static RAM [2]. The major subsystems of the solver are the row decoder, the column decoder, the output buffer, the boundary cells, and the 14 x 14 array of interior resistive cells.

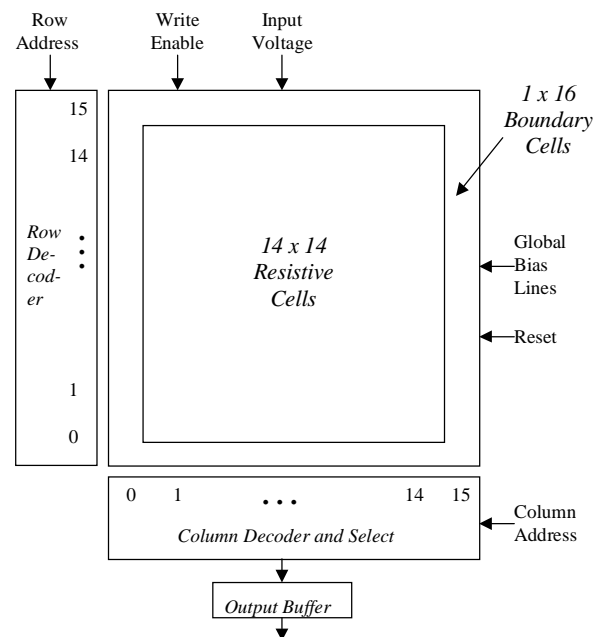


Figure 2 Chip floorplan.

Fig. 3 shows the schematic of the interior resistive cell. A sample and hold circuit stores the input voltage on an input capacitor. An operational transconductance amplifier converts the input voltage into a bi-directional current. That current is injected onto the cell node and its effect is spread to four nearest neighbors through CMOS resistors biased in the ohmic region. The output voltage is sampled using a source follower. The cell can be reset to ground via a reset line, in order to be able to compensate for the DC offset voltage in the source follower. A final feature of the interior cell is that it is possible to inject a static DC current through a current mirror for testing the array.

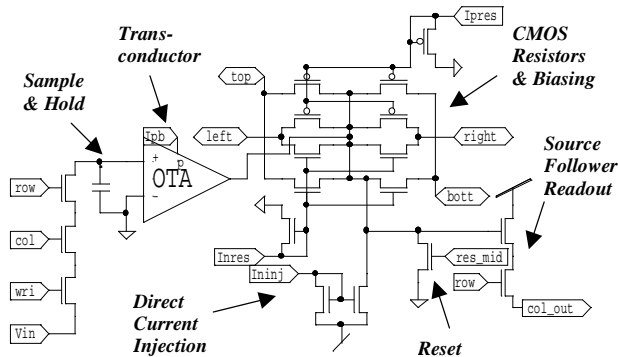


Figure 3 Schematic of interior resistive cell.

The circuit of a boundary cell is shown in Fig.4. The purpose of the boundary cell is to fix the voltage along the boundary of the array. An opamp configured as a follower is used to clamp the cell node voltage. A reset line is at the input of the opamp, in order to be able to compensate for the DC offset in the opamp.

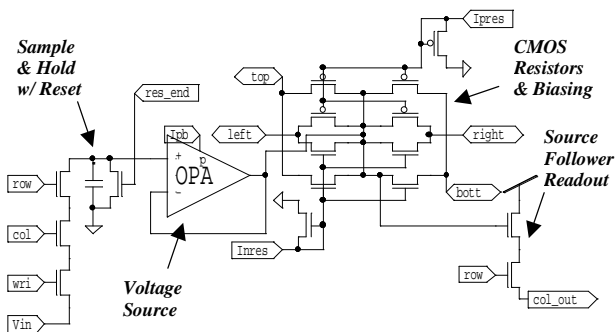


Figure 4 Schematic of boundary cell.

3. Measurements

An 8 x 8 static Poisson-equation solver is previously described in [3]. Data measured from one chip is shown in Fig. 5. A constant current of 0.1 μA is injected into each node. A small-signal resistance of 200 k Ω exists between neighboring cells. The boundary voltages are all

fixed at 0 V. From Fig. 5 we see the characteristic bowl shape, as expected.

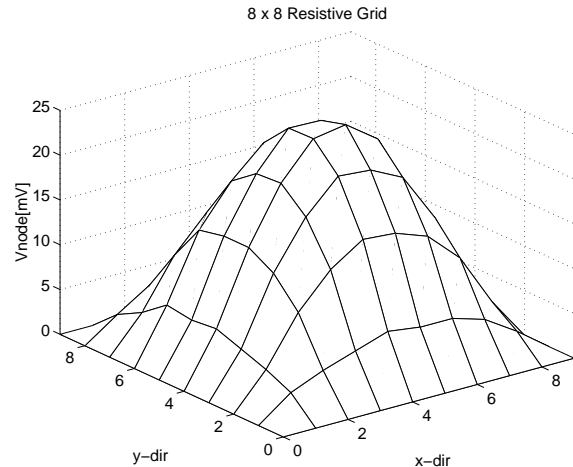


Figure 5 Data measured from a static 8 x 8 Poisson-equation solver chip. The small-signal resistance between each cell is 200k Ω . A constant current of 0.1 μA was injected into each cell.

4. Acknowledgements

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References

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- [3] P.M. Furth and N. Clark, "A Two-Dimensional Poisson-Equation Solver Implemented in Analog VLSI," *Proc. 7th NASA Symp. VLSI Design*, Albuquerque, NM, October 1998.