

EE 361 Digital Design II

Spring, 2005

Time	Tuesday & Thursday 8:55 – 10:20 Thomas and Brown Hall, room 204
Instructor	Dr. Krist Petersen Thomas & Brown, room 106 (505) 646-3117 kpeterse@nmsu.edu
Office Hours	Monday & Friday 10:30 – 11:30 AM
Course Description	Sequential design techniques. Classical and modern design of synchronous and asynchronous machines. Designs using SSI and MSI technology.
Prerequisite	A grade of 'C', or better, in EE 261
Required Materials	<u>Fundamentals of Digital Logic with VHDL Design</u> , by Brown and Vranesic. (either edition)
Recommended Materials	<u>TTL Logic Data Book</u> , By Texas Instruments
Web Address	www.ece.nmsu.edu/~kpeterse/EE361
Objectives	Upon completion of EE 361 a students will be able to: Draw a synchronous state diagram which solves a given problem. Design a minimal synchronous state table from a state diagram. Create a race-free synchronous schematic from a state table. Design simple asynchronous solutions. Use registers, counters, and shifters. Use a CAD tool to design and simulate sequential digital logic. Write VHDL descriptions of sequential logic expressions. Design and implement practical solutions to realistic word problems.
Relationship of the Course to Program Objectives	EE 361 serves as a breadth elective, providing a continuation of the material covered in EE 261. The student is exposed to sequential digital logic systems, the basis for all modern designs, including computers. As such, EE 361 is relevant to all areas of Electrical and Computer Engineering. Upon completion of EE 361, students may continue their computer engineering education by enrolling in EE 466, Modern Digital System Design.

Grading

Grades will be based on 4 in-class exams plus a final. Exams are cumulative, however emphasis will be placed on the material covered since the last exam. The lowest exam grade will be replaced by a copy of the final exam score, unless the final is the lowest. Thus, you may miss one exam with no detrimental effects. You may not miss the final. No make-up exams will be given.

Homework will be assigned, but not collected or graded. Solutions will be posted. The exam questions will be similar to the homework, so doing the assignments is good practice for the exams.

A grade of 'I' (incomplete) will only be issued in circumstances, beyond the student's control, which prevent completion of the required work. Any request for a grade of 'I' must be documented, and the cause(s) must occur after March 9, 2005. A student must have been passing the class on June March 9, 2005 in order to qualify for an 'I'.

A grade of 'W' (withdrawn) will only be issued prior to March 9, 2005.

Attendance

No attendance will be taken in lecture. However, inasmuch as the quizzes are unannounced, it will behoove you to attend lecture on a regular basis. Attendance will be taken in lab. Failure to attend lab will result in automatic failure of the class, regardless of other grades.

Academic Dishonesty

Departmental policy states students found guilty of academic dishonesty (copying, plagiarism, unauthorized collaboration or references, etc.) will be suspended from the university. Cell phones, PDA's, computers, and other electronic devices which support communications and/or data storage may not be brought into the classroom during exams (including the final) unless expressly allowed. The use of such devices during an exam is considered academic dishonesty and will be dealt with accordingly.

Students with Disabilities

If you have or believe you have a disability, you may wish to self-identify. You can do so by providing documentation to the Office for Services for Students with Disabilities, located at Garcia annex (phone 646-6840). Appropriate accommodations may then be provided for you. If you have a condition which may affect your ability to exit safely from the premises in an emergency or which may cause an emergency during class, you are encouraged to discuss this in confidence with the instructor and/or the director of Disabled Student Programs. If you have general questions about the Americans with Disabilities Act (ADA), call 646-3635.

Topics Covered

Note: the topics below may not be covered in the order shown.

- Sequential circuits
- Binary cell
- Synchronous vs asynchronous
- State descriptions
- State tables
- State diagrams
- Mealy vs Moore machines
- State reduction
- Describing state machines in VHDL
- Block diagram of a finite state machine
- Clocking
- State machine timing
- Next state logic
- State memory
- Output logic
- Analysis of sequential circuits
- Standard flip-flop types
- Using MUX's as combinational logic
- Using DMUX's as combinational logic
- Registers
- Shifters
- Optimal state code assignment
- Counters
- Using PLAs as combinational logic
- Using ROM's as combinational logic
- Designing state machines using PLD's.