

EE 361 Digital Design II

Summer I, 2004

- Time** Monday-Friday 8:25 – 9:55 PM
Thomas and Brown Hall, room 204
- Instructor** Dr. Krist Petersen
Goddard Tower, room 102
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- Office Hours** Monday-Friday 10:30 –11:30 AM
- Course Description** Sequential design techniques. Classical and modern design of synchronous and asynchronous machines. Designs using SSI and MSI technology.
- Prerequisite** A grade of `C`, or better, in EE 261
- Required Materials** Fundamentals of Digital Logic with VHDL Design, by Brown and Vranesic.
- Recommended Materials** TTL Logic Data Book, By Texas Instruments
- Grading** Grades will be based on 4 in-class exams. Exams are cumulative, however emphasis will be placed on the material covered since the last exam. The lowest exam grade will be replaced by a copy of the final exam score, unless the final is the lowest. Thus, you may miss one exam with no detrimental effects. You may not miss the final. No make-up exams will be given.
- Homework will be assigned, but not collected or graded. Solutions will be posted. The exam questions will be similar to the homework, so doing the assignments is good practice for the exams.
- A grade of `I` (incomplete) will only be issued in circumstances, beyond the student's control, which prevent completion of the required work. Any request for a grade of `I` must be documented, and the cause(s) must occur after June 10, 2004. A student must have been passing the class on June 10, 2004 in order to qualify for an `I`.
- A grade of `W` (withdrawn) will only be issued prior to June 10, 2004.

Topics Covered

Note: the topics below may not be covered in the order shown.

- Sequential circuits
- Binary cell
- Synchronous vs asynchronous
- State descriptions
- State tables
- State diagrams
- Mealy vs Moore machines
- State reduction
- Describing state machines in VHDL
- Block diagram of a finite state machine
- Clocking
- State machine timing
- Next state logic
- State memory
- Output logic
- Analysis of sequential circuits
- Standard flip-flop types
- Using MUX's as combinational logic
- Using DMUX's as combinational logic
- Registers
- Shifters
- Optimal state code assignment
- Counters
- Using PLAs as combinational logic
- Using ROM's as combinational logic
- Designing state machines using PLD's.