

Course: E.E. 361, Digital Design II
 Summer II, 2002
 M-F, 8:30 am - 9:55 am
 Thomas & Brown Hall, Room 303

Description: Digital logic design techniques, design of synchronous and asynchronous sequential machines using both classical and modern techniques.

Instructor: A. K. Petersen
 Thomas & Brown Hall, Room 312
 646-4932

Prerequisite: EE 111 and EE 261

Office Hours: M-F, 10:00 am - 10:30 am

Texts: Fundamentals of Digital Logic with VHDL Design, By Brown and Vranesic

References: TTL Logic Data Book, By Texas Instruments

Grading:

Exams	75%	A	>92	
Homework	25%	B	84-92	
		C	75-83	S >74
		D	67-74	
		F	<67	U <75

Exams: All exams (including the final) will be weighted equally. If your final exam is not your lowest score, the lowest score will be replaced by a copy of your final exam score. If your final exam score is your lowest, no adjustment will be made. Therefore, you must take the final, but one of the other exams may be missed. **NAMES ON ALL EXAMS MUST BE WRITTEN IN INK !!** No make-up exams will be given.

Homework: Homework will be assigned periodically. Many assignments will require the use of a computer. If you do not have a computer at home, you may use those in room 201 or 202. Late homework is not accepted.

Cheating: Departmental policy states students found guilty of cheating (copying, plagiarism, unauthorized collaboration or references, etc.) will be suspended from the university.

Attendance: No role will be taken in lecture.

Lecture Schedule

7/3	Binary Cell, Sequential vs Combinational
7/5	RS Latch, Synchronous vs Asynchronous, Block Diagram
7/8	States, State Table, State Diagram, and Excitation Tables
7/9	D Flip Flop Design, T Flip Flop Design <i>Last day to register, add, or file a degree application</i>
7/10	JK Flip Flop Design, Moore vs Mealy Machines, Set-up & Hold Time
7/11	Parity Generator
7/12	Exam #1
7/15	3 Bit Framing Code Detector
7/16	3 Bit Sequential Code Detector
7/17	Mealy Machine Example, State Reduction
7/18	State Reduction, State Code Assignment
7/19	Exam #2
7/22	Waveform Generator
7/23	Register Design, FSM Design using Registers <i>Last day to drop with a `W`</i>
7/24	Counter Design, FSM Design using Counters
7/25	Shifter Design, FSM Design using Shifters
7/26	Exam #3
7/29	FSM Design using Memories, FSM Design using Microprocessors, Pop Drop Design
7/30	Pop Drop Design
8/31	One Hot Controllers, Pseudo-Synchronous Machines
8/1	Gated Pulse Generator Example, Timing Description, Primitive State Assignment, Primitive State Flow Diagram <i>Last day to withdraw from the university</i>
8/2	Exam #4
8/5	Merged Primitive State Diagram
8/6	Switch Debouncer Example
8/7	Pulse Generator Example
8/8	Hazards
8/9	Final Exam